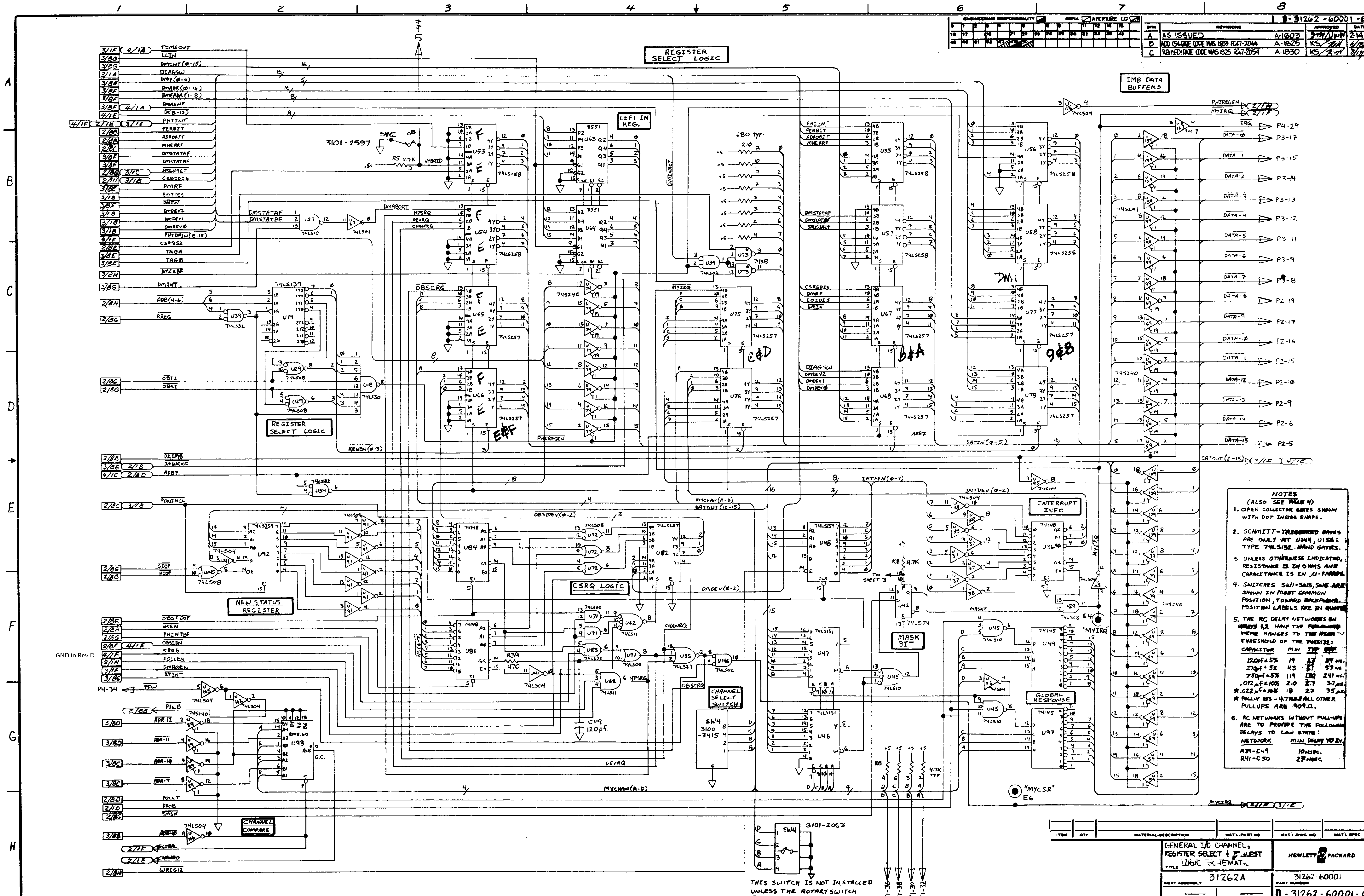


D-31262-60001-6

SYM	REVISIONS		APPROVED	DATE
A	AS ISSUED	A-1803	[illegible]	2-14-78
B	ADD C54 DATE CODE WAS 1803 RC47-2044	A-1825	KS	6/18/78
C	REVISED DATE CODE WAS 1825 RC47-2054	A-1830	KS	8/17/78

NOTES
(ALSO SEE PAGE 4)

1. OPEN COLLECTOR GATES SHOWN WITH DOT INSIDE SHAPE.
2. SCHMITT-TRIGGERED GATES ARE ONLY AT U144, U156: TYPE 74LS132 NAND GATES.
3. UNLESS OTHERWISE INDICATED, RESISTANCE IS IN OHMS AND CAPACITANCE IS IN μ-FARADS.
4. SWITCHES SW1-SW3, SW5 ARE SHOWN IN MOST COMMON POSITION, TOWARD BACKPLANE. POSITION LABELS ARE IN QUOTES.
5. THE RC DELAY NETWORKS ON SHEETS 1,2 HAVE THE FOLLOWING TIME RANGES TO THE [illegible] THRESHOLD OF THE 74LS132:

CAPACITOR	MIN	TYP	MAX
120pf ± 5%	19	27	39 ns.
270pf ± 5%	43	[illegible]	87 ns.
750pf ± 5%	119	[illegible]	241 ns.
.012 μF ± 10%	2.0	2.7	3.7 μs.
★ .022 μF ± 10%	18	27	35 μs.

★ PULLUP RES = 4.7K; ALL OTHER PULLUPS ARE 909Ω.

6. RC NETWORKS WITHOUT PULL-UPS ARE TO PROVIDE THE FOLLOWING DELAYS TO LOW STATE:

NETWORK	MIN DELAY TO [illegible]
R39-C49	10 NSEC.
R41-C50	23 NSEC.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: GENERAL I/O CHANNEL, REGISTER SELECT & REQUEST LOGIC SCHEMATIC

HEWLETT PACKARD

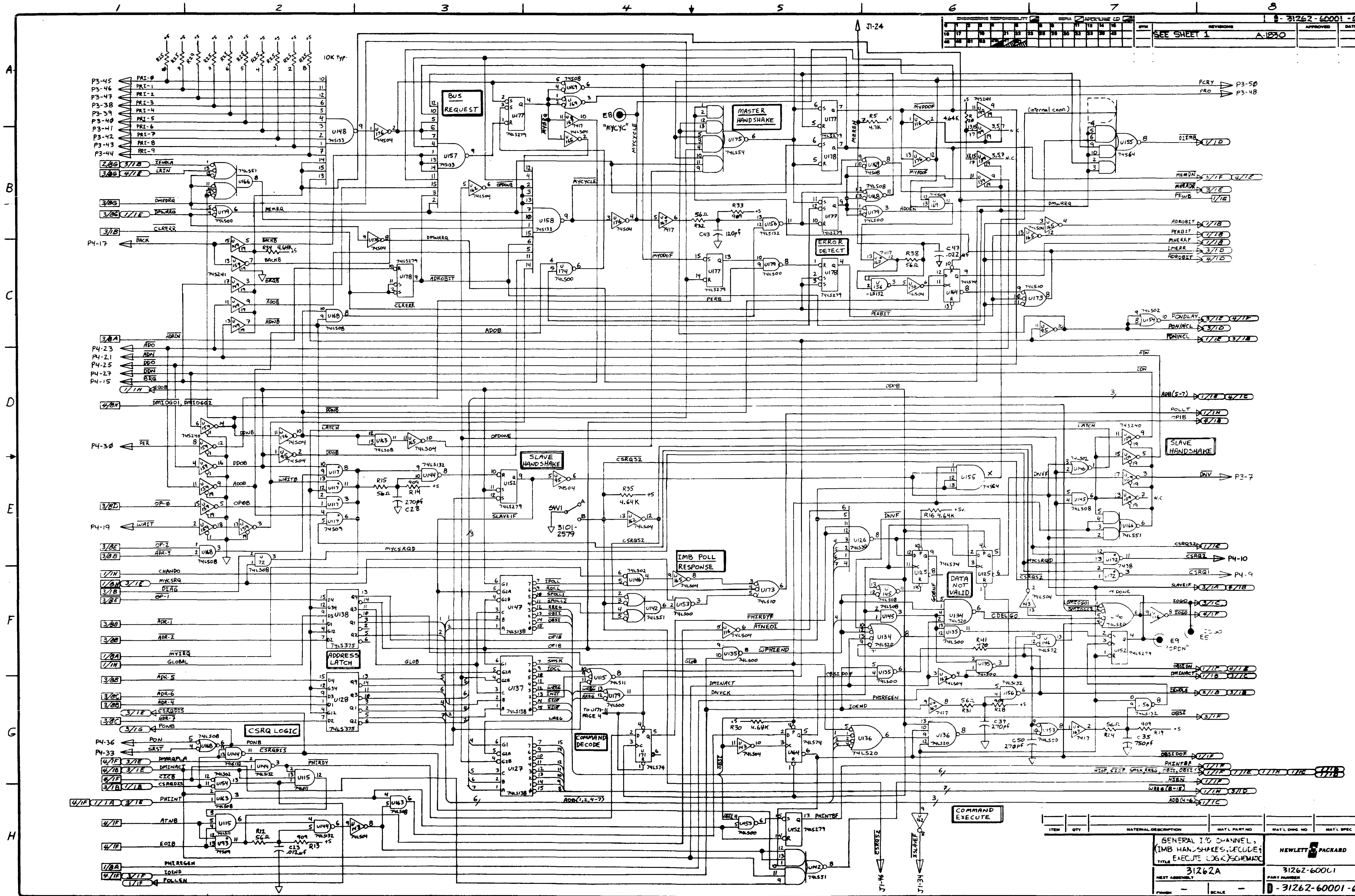
NEXT ASSEMBLY: 31262A

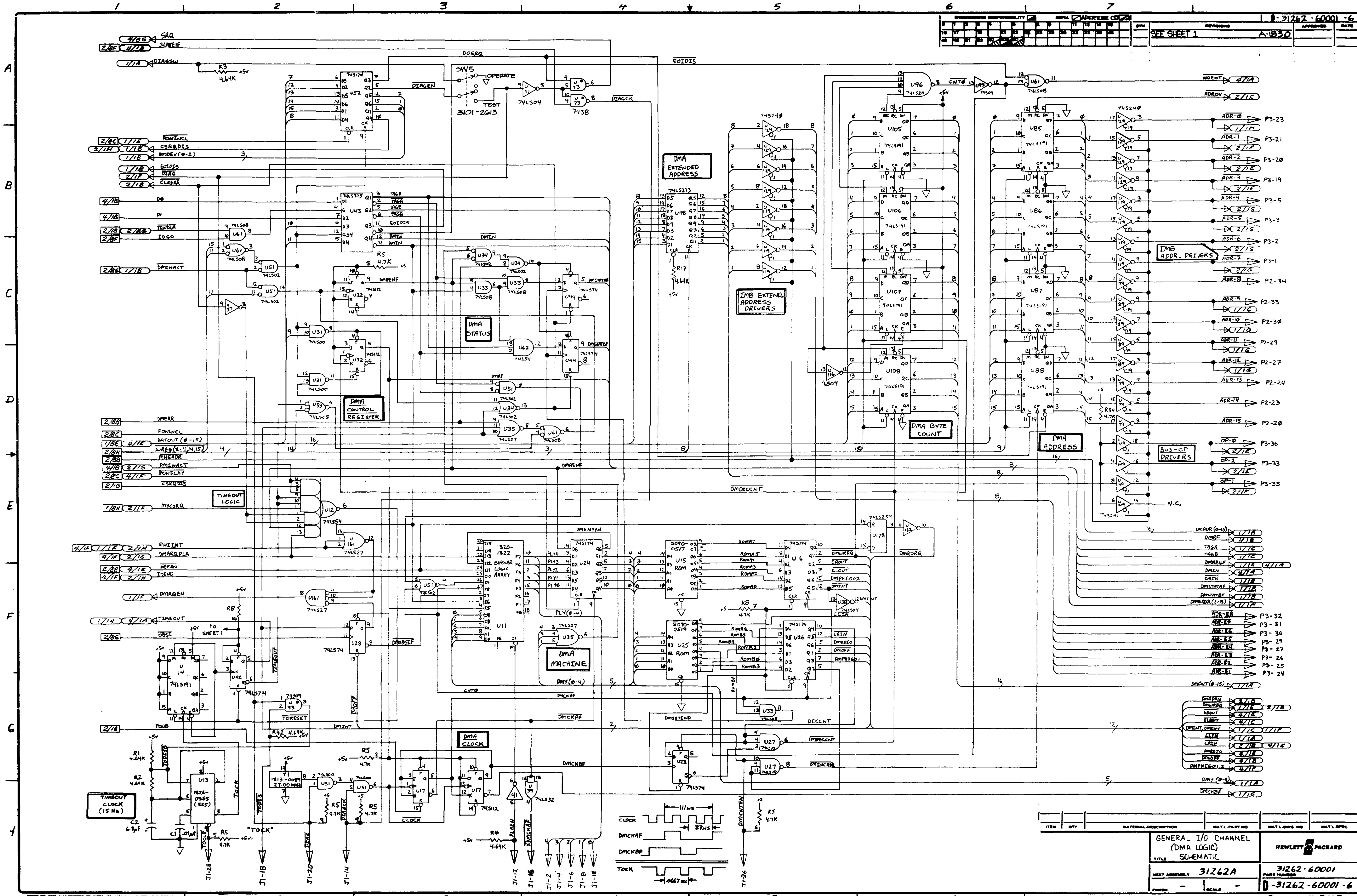
PART NUMBER: 31262-60001

FINISH: — SCALE: —

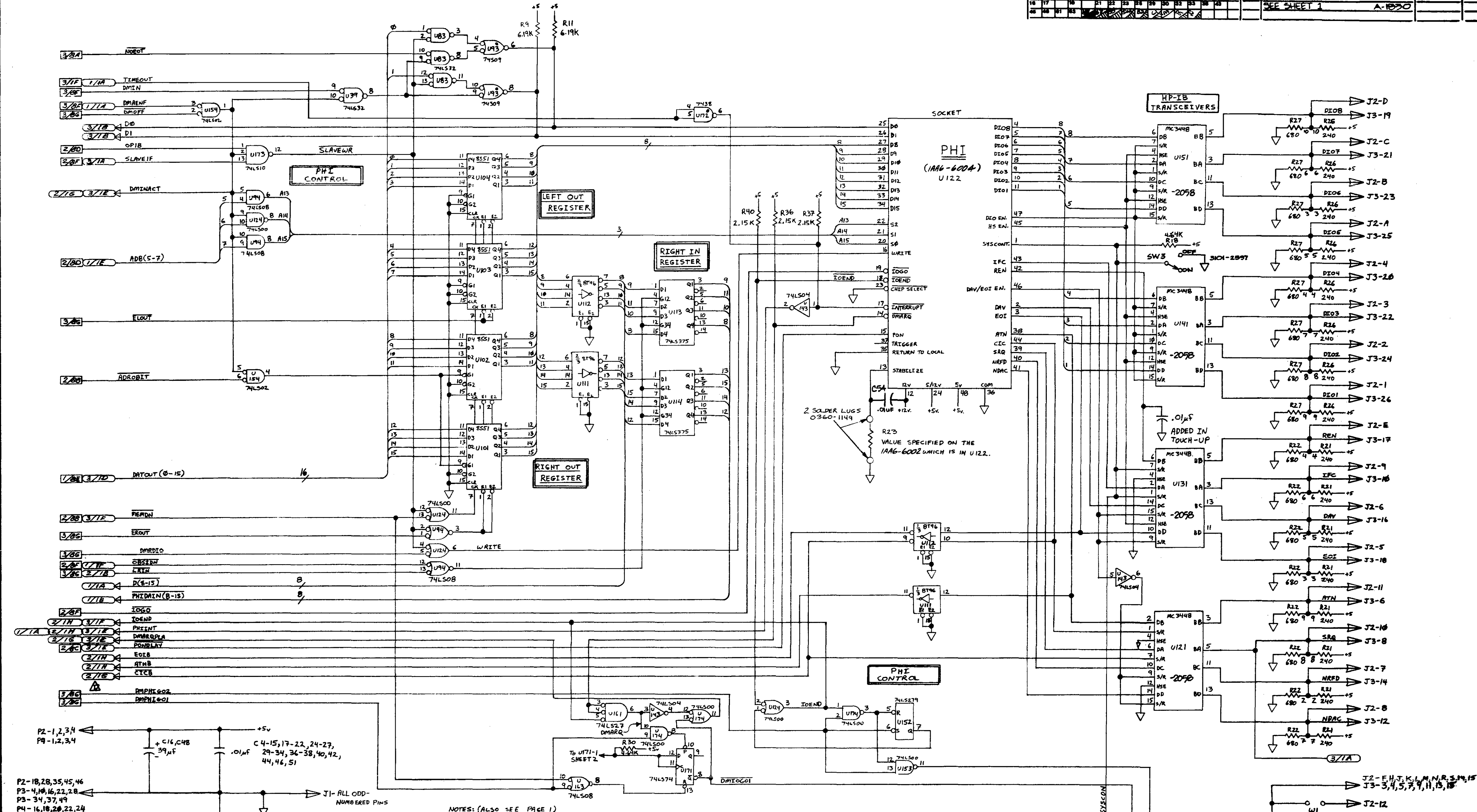
D-31262-60001-6

SHEET 1 OF 5


BUS REQUEST
MASTER HANDSHAKE
ERROR DETECT
SLAVE HANDSHAKE
IMB POLL RESPONSE
DATA NOT VALID
ADDRESS LATCH
COMMAND DECODE
CSRQ LOGIC
COMMAND EXECUTE
"MYCYC"
SEE SHEET 1
A-1830
GENERAL I/O CHANNEL, (IMB HANDSHAKES, DECODE, EXECUTE LOGIC) SCHEMATIC
31262A
31262-60001
HEWLETT PACKARD
D-31262-60001-6
SHEET 2 OF 5


GENERAL I/O CHANNEL
(DMA LOGIC)
SCHEMATIC
31262A
31262-60001
D-31262-60001-6
SHEET 3 OF 5
HEWLETT PACKARD
SEE SHEET 1
A-1830
DMA EXTENDED ADDRESS
IMB EXTEND. ADDRESS DRIVERS
DMA STATUS
DMA CONTROL REGISTER
DMA BYTE COUNT
DMA ADDRESS
IMB ADDR. DRIVERS
BUS-CP DRIVERS
TIMEOUT LOGIC
DMA MACHINE
DMA CLOCK
TIMEOUT CLOCK (15 Hz)

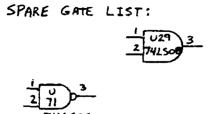
Revisions: SEE SHEET 1 — A-1830



8. RESISTOR AND CAPACITOR DESIGNATORS NOT USED: R6, R7, C3, C41.

9. OFFPAGE SYMBOLS ARE SQUARED TO INDICATE ON WHICH SHEET THE SIGNAL IS SOURCED. SIGNALS SOURCED ON A PAGE HAVE AN ARROW POINTING TOWARD THE OFFPAGE SYMBOL.

7. SPARE GATE LIST:



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-ENG. NO.	MAT'L-SPEC.

TITLE: GENERAL I/O CHANNEL (HP-IB INTERFACE) SCHEMATIC

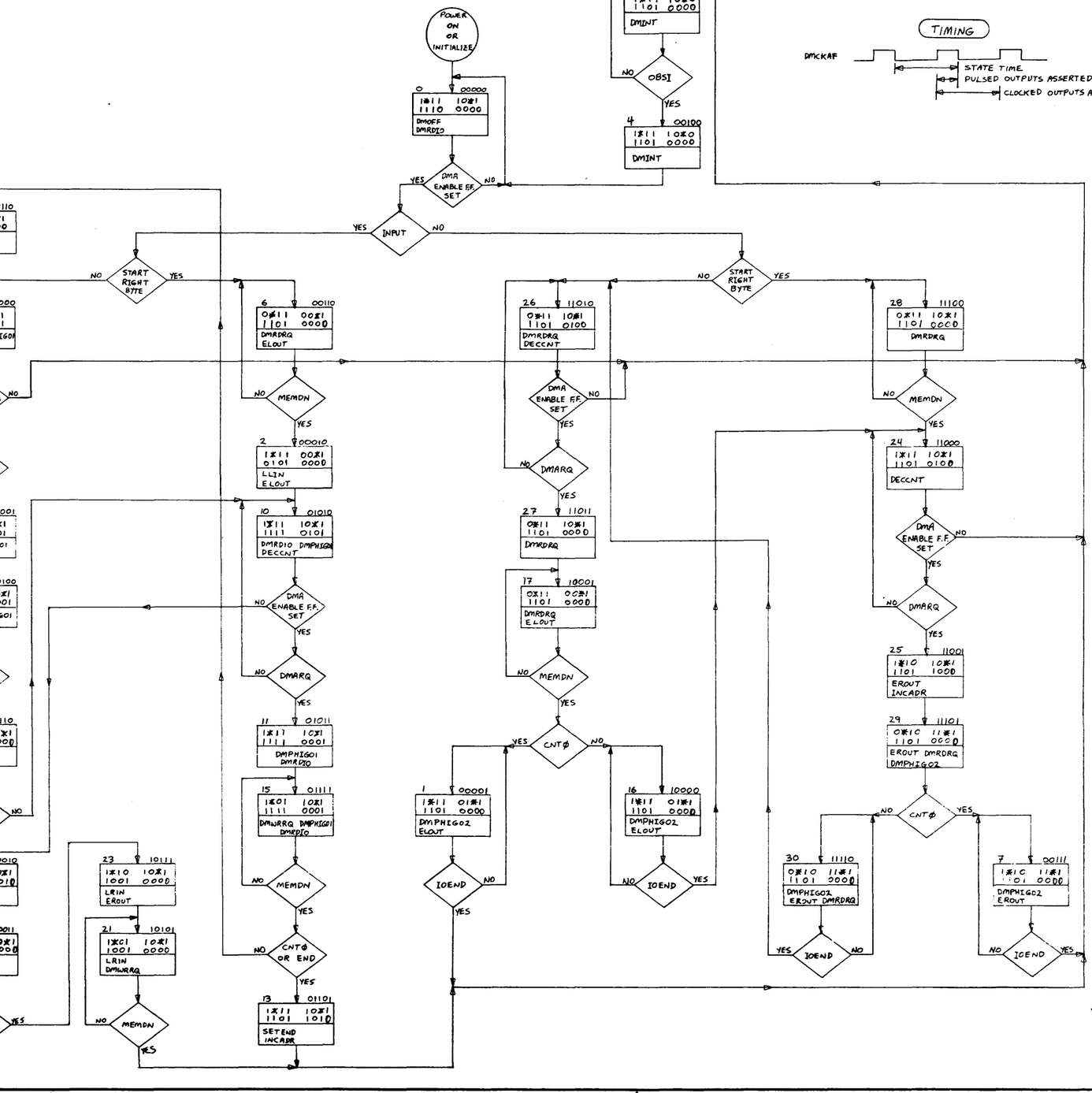
HEWLETT PACKARD

NEXT ASSEMBLY: 31262A

PART NUMBER: 31262-60001

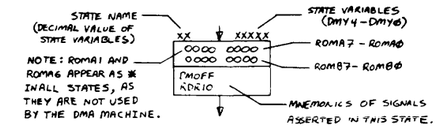
FINISH: - SCALE: -

D-31262-60001-6



TIMING

LEGEND



MNEMONICS

• INPUTS

CNTØ	≡	BYTE COUNT REGISTER EQUALS ZERO.
DMARQ	≡	INPUT: INBOUND FIFO NOT EMPTY. OUTPUT: OUTBOUND FIFO NOT FULL.
IOEND	≡	PHI HANDSHAKE COMPLETED.
MEMDN	≡	MEMORY OPERATION COMPLETED.
OBSI	≡	IMB "OBSI" COMMAND HAS BEEN DONE.
TAG	≡	TAG BITS DØ,D1 OF PHI INDICATE END OF TRANSFER.

• OUTPUTS

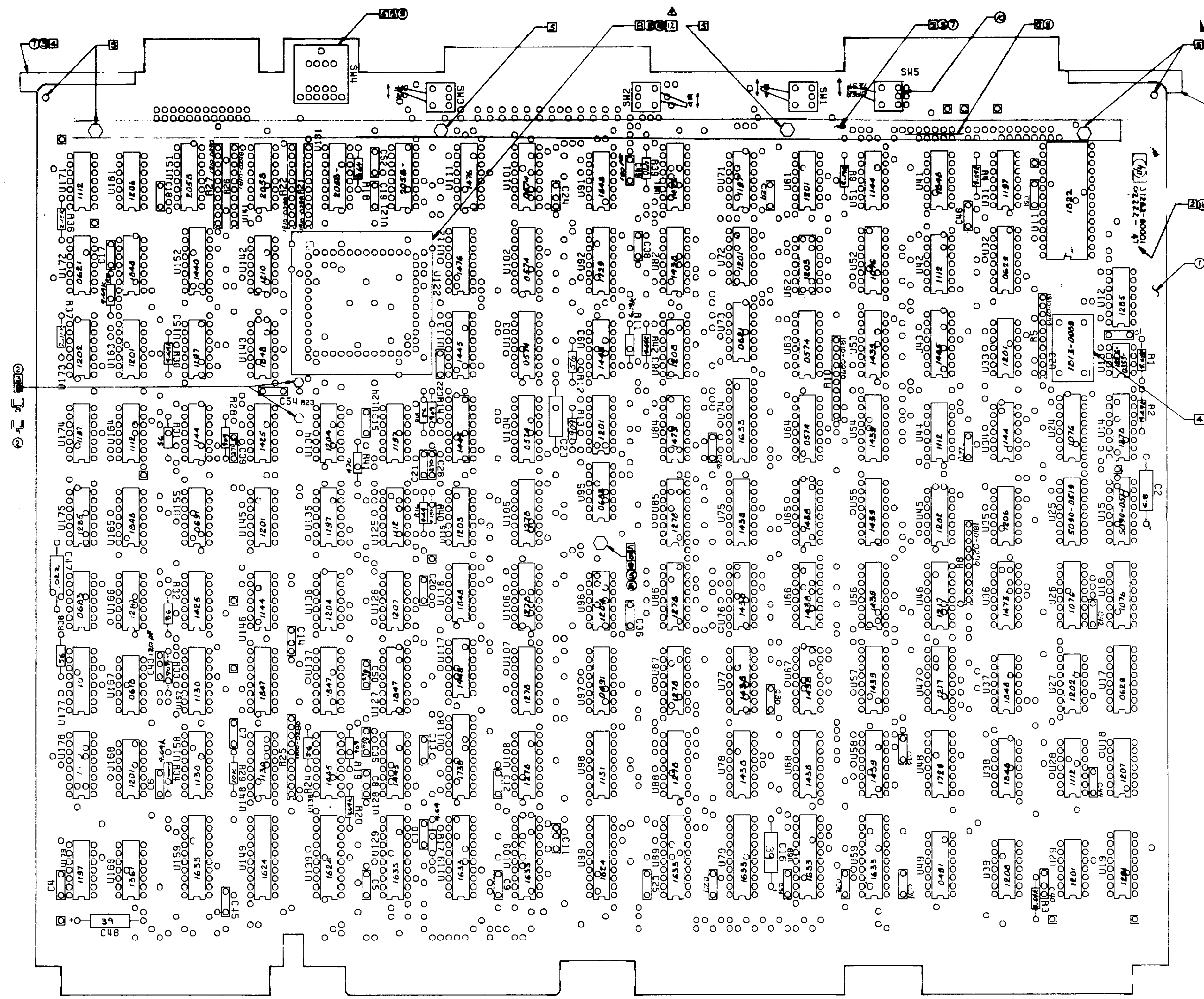
DECCNT	≡	DECREMENT BYTE COUNT AND COMPLEMENT LEFT/RIGHT BIT ONCE IN THIS STATE.
DMINT	≡	ASSERT CSRQ. AFTER OBSI, CSRQ IS HELD OFF.
DMPHIGO1	≡	START WRITE TO PHI. THIS WILL PROVIDE A "FAST" PHI HANDSHAKE WHICH RELEASES IOGO AS SOON AS IOEND IS ASSERTED, ASYNCHRONOUS TO DMA MACHINE.
DMPHIGO2	≡	START READ FROM PHI. THIS PROVIDES A PHI HANDSHAKE WHICH RELEASES IOGO AS SOON AS MEMDN IS ASSERTED, ASYNCHRONOUS TO DMA MACHINE.
DMOFF	≡	DMA IS IDLE: RE-ENABLE ALL CSRQ'S AND ALLOW SLAVE ACCESS TO PHI.
DMRDIO	≡	SELECT PHI TO READ FIFO. IT IS SELECTED TO WRITE TO FIFO OTHERWISE. IN STATE Ø, THE SLAVE MAY OVERRIDE DMRDIO.
DMRDRQ	≡	REQUEST READ OF MEMORY.
DMWRRQ	≡	REQUEST WRITE TO MEMORY. THE CYCLE WILL NOT START UNTIL IOEND OR LRIN IS ASSERTED.
ELOUT	≡	GATE THE LEFT BYTE OUTPUT REGISTER TO THE PHI DATA LINES.
EROUT	≡	GATE THE RIGHT BYTE OUTPUT REGISTER TO THE PHI DATA LINES.
INCADR	≡	INCREMENT THE DMA ADDRESS REGISTER.
LLIN	≡	CLOCK PHI DATA LINES INTO LEFT BYTE INPUT REGISTER EACH STATE TIME AT DMCKAF↓.
LRIN	≡	LATCH PHI DATA LINES INTO RIGHT BYTE INPUT REGISTER.
SETEND	≡	SET DMA STATUS TO APPROPRIATE TERMINATION CODE.

NOTES

1. OUTPUTS OCCURRING IN CONSECUTIVE STATES DO NOT GLITCH BETWEEN STATES, EXCEPT LLIN, WHICH IS TAKEN DIRECTLY FROM THE DECODER ROM.
2. THESE INPUTS ARE ASYNCHRONOUS: IOEND, MEMDN, DMARQ, OBSI.
3. THE ONLY PULSED OUTPUTS ARE: DECCNT, SETEND.
4. BOTH OUTPUT DATA REGISTERS ARE LOADED AT OCCURRENCE OF MEMDN.
5. THE HP-IB "END" MESSAGE IS SENT IN STATES 7,16 UNLESS INHIBITED WITH A DMA CONTROL BIT.
6. MEMDN REMAINS ASSERTED UNTIL BOTH DMRDRQ AND DMWRRQ ARE NOT ASSERTED.
7. ONCE DMRDRQ IS ASSERTED, THE MEMORY CYCLE WILL COMPLETE EVEN IF DMRDRQ IS REMOVED BEFORE MEMDN.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: GENERAL I/O CHANNEL (DMA MACHINE FLOWCHART) SCHEMATIC	HEWLETT PACKARD
NEXT ASSEMBLY: 31262A	PART NUMBER: 31262-60001
FINISH: - SCALE: -	D-31262-60001-6



F-31262-60001-18

LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]
B	REVISED NOTE 2 & ADDED ITEM [illegible]	[illegible]	[illegible]
C	[illegible]	[illegible]	[illegible]
D	ADDED ITEM 16 TO DATE CODE CALLOUT. DOC CHG.	[illegible]	[illegible]
E	REMOVED test Pins (4 PLCS); 47-3902	BC	[illegible]
F	ADDED NOTE 12 PER DOC. CHG.	MH	[illegible]
G	R36, 37 & 40 WAS 2.51K IN ERROR. C49 WAS 180pF IN ERROR. Added various HP [illegible] to Component list [illegible] 47-3416	BC	7-2[illegible]
H	ADDED 270pF to C39; C24 [illegible] Doc Chg	BC	3-2-[illegible]

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS.
   ALL RESISTORS 1/4 W 1% MF,
   EXCEPT 56Ω & 470 ARE 5%.
   ALL CAPACITANCE IN MICROFARADS.
   ALL CAPACITORS ARE .01 CER DISC.
   ALL SWITCHES ARE 3101-2597
   ALL I.C.'S ARE 1820-

[2] INSTALL ITEM (16)

[3] INSTALL & RIVET ITEM (2) 2 PLACES PRIOR TO LOADING ANY COMPONENTS. ORIENTATION AS SHOWN AT LEFT OF NOTATION SYMBOL.

[4] ORIENT Y1 WITH MANUFACTURER ORIENTATION SYMBOL AT LOWER RIGHT. BODY OF ITEM (12) MUST BE SPACED FROM BOARD WITH BEADS. ITEM (13) OR SELF CONTAINED SPACERS

[5] MASK AS INDICATED PRIOR TO WAVE SOLDER

[6] USE SUPPORT FIXTURE DURING WAVE SOLDER.

[7] INSTALL ITEMS (3), (4) & (6) IN P.C. FINAL ASSEMBLY.

[8] INSTALL ITEM (11) IN U122 AFTER DTS-70 TEST. & SOLDER R23 RES. OF VALUE STAMPED ON (11) ACROSS THE TWO ITEMS (15). USE ANTI STATIC PROTECTION BEFORE HANDLING ITEM (11).

9 SERIALIZE BOARD

10 SCHEMATIC D-31262-60001-16.

11 ITEM (14) NEAR HP LOGO.

△ [12] NOTE: R23 RES. VALUE MAY NOT MATCH VALUE STAMPED ON ITEM [illegible] AFTER SYSTEM TEST IS COMPLETE.

ITEM	QTY	MATERIAL DESCRIPTION	MATL-PART NO.	MATL DWG NO	MATL SPEC
16		LABEL - DATE CODE	9320-5320		
15	2	SOCKET CLIPS	1200-0844		
14	1	LABEL, WARRANTY	7120-6830		
13	4	BEAD SPACER	4330-0145		
12	1	I.C. DIGITAL (Y1)	1813-0088		
11	1	PHI	1AA6-6004		
10	1	SWITCH	3101-2613		
9	1	SWITCH, THWAL 16 POS	3100-3415		
8	1	LABEL	7120-6600		
7	1	BRACE, PC BOARD	5040-6058		
6	1	SPACER	5020-7318		
5	5	SCREW 4-40 X .31	[illegible]-0077		
4	2	EXTRACTOR	5040-6008		
3	2	PIN GRV. .062 X .250	1480-0116		
2	2	[illegible], SOLDER TERM.	0360-1148		
1	1	[illegible], ETCHED	31262-80001		

PROCESS REVIEW
DATE 2/1/84

GENERAL I/O CHANNEL ASSY

NEXT ASSEMBLY: 31262A

PART NUMBER: 31262-60001

SCALE 2/1

F-31262-60001-18

HEWLETT PACKARD